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(54) **Semiconductor pressure sensor with single-crystal silicon diaphragm and single-crystal gage elements and fabrication method therefor**

Halbleiter-Druckwandler mit Einkristall-Silizium-Membran und Einkristall-Dehnungsmessstreifen und Herstellungsverfahren dazu

Capteur semi-conducteur de pression avec membrane en silicium monocristallin et jauges de contraintes monocristaux et son procédé de fabrication

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US-A- 4 970 487 **US-A- 5 095 401**

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Description

Background

[0001] This invention relates to a method for manufacturing semiconductor pressure sensors.

[0002] Semiconductor pressure sensors and strain gages are commonplace today. Their extremely small size, less than 0.125 inch (3.175 mm) in any dimension, is typical. High durability to outside forces makes these devices popular for the pressure measurement needs of hydraulic and aerodynamics forces, among other applications.

[0003] Typically, semiconductor pressure sensors contain a diaphragm of one or more silicon layers for deflecting in response to opposing pressure environments, and piezoresistive elements that are configured for sensing the direction and/or magnitude of diaphragm deflection.

[0004] The manufacture of these sensors makes the diverse range of devices available today and one aspect of the invention provides improvements in that manufacture. Because high temperature stability is often required, improvements relating to sensor heat stability is an active research area. Dielectric isolation is one technique which increases stability. The dielectric ideally isolates semiconductor piezoresistive elements from the diaphragm, the support structure, and other piezoresistive elements. Silicon dioxide, SiO₂, exemplifies a known dielectric that maintains a nearly constant resistance over significant temperature changes.

[0005] The type of silicon used in the pressure sensor is also important. Single-crystal silicon and polycrystalline silicon materials have different properties that influence mechanical strength, sensitivity, and even manufacturability.

[0006] Despite the advances made in semiconductor physics, pressure sensors with improved temperature stability and higher pressure sensitivity are sought, particularly for use in hostile environments. Devices available today generally have limited sensitivity and dielectric isolation, that restrict stability and high temperature operation.

[0007] In U.S. Patent No. 4,672,354 for "Fabrication of Dielectrically Isolated Fine Line Semiconductor Transducers and Apparatus", for example, glass is used as an insulator and as a bonding agent. Such a pressure transducer is difficult to manufacture, and has other undesirable characteristics.

[0008] US-A-5,094,401 discloses the fabrication of diaphragm pressure sensors utilizing silicon-on-insulator technology.

[0009] With this background, an object of this invention is to provide improved semiconductor pressure sensors and associated manufacturing methods, and in particular, for uses which require high temperature stability and high sensitivity.

[0010] Another object of the invention is to provide a

high sensitivity semiconductor pressure sensor which is easier to manufacture than competitive existing sensors.

[0011] A further object of this invention is to provide a semiconductor pressure sensor, and a related method of manufacture, for dielectrically isolating single crystal silicon sensors, and further for creating a controllable etch stop configuration for forming the diaphragm.

[0012] Other objects of the invention are evident in the description which follows.

Summary of the Invention

[0013] The invention features a method for manufacturing semiconductor pressure sensors. A silicon-on-insulator (SOI) wafer is provided to include a substrate, a silicon oxide implantation which functions as an etch stop, and surface annealed silicon. Epitaxial silicon is grown on the surface silicon to form a single-crystal silicon diaphragm with opposed first and second surfaces. The diaphragm is afterwards implanted by a second silicon oxide layer to form a dielectric isolator. The second silicon oxide layer is annealed to provide surface silicon for a piezoresistive gage element made of p-type implants. The piezoresistive gage element is formed within the surface annealed silicon by boron implantation and by etching to create a dielectrically isolated piezoresistive sensing element. It is preferably provided with additional dielectric isolation by nitride deposition. Evaporated metal, e.g., aluminum, is deposited and etched to provide an external electrical connection to the piezoresistive gage element. The substrate, as part of the SOI wafer, is then etched to provide a backside pressure port such that the diaphragm can deflect in response to a pressure difference between the first and second surfaces.

[0014] Alternatively, the silicon oxide implantation which forms the etch stop is confined to a localized and buried volume within the silicon substrate, to form both an etch stop and an over-range cavity support region. Oxygen ion implantation is implanted locally by masking portions of the silicon substrate. Once the buried implantation is complete, the substrate silicon is epitaxially grown to form a single-crystal silicon diaphragm and piezoresistive gage element, as above.

[0015] The features of the method for manufacturing a sensor according to the invention provide several advantages. In particular, the dielectric isolation of the silicon oxide layer provides the sensor with high operating stability and high temperature capability, and also provides an etch stop for backside etching of the pressure port. By using single-crystal silicon as the piezoresistive gage elements, the sensor provides relatively high sensitivity and low pressure differentials, and is relatively easy to manufacture. This enables the device to be coupled more effectively with digital electronics, with the potential for solving other high-performance, intelligent pressure transmitter needs. Further, the cavity formed

by localized oxygen implantation and etching provides an over-range stop for the diaphragm, resulting in high robustness.

[0016] These and other aspects will become apparent in the following description.

Brief Description of the Drawings

[0017] For a fuller understanding of the nature and objects of the invention, reference should be made to the following detailed description and the accompanying drawings, in which:

FIGURE 1 is a cross-sectional view of a semiconductor pressure sensor constructed in accordance with the invention;

FIGURE 1A is a schematic top view of the pressure sensor of FIGURE 1;

FIGURE 2 is a cross-sectional view of an illustrative silicon-on-insulator (SOI) wafer for the fabrication of the sensor of FIGURE 1;

FIGURE 2A shows the SOI wafer of FIGURE 2 with epitaxially grown silicon to create a single-crystal silicon diaphragm;

FIGURE 2B shows the wafer of FIGURE 2A with additional oxide implantation and surface annealed silicon;

FIGURE 2C shows the wafer of FIGURE 2B implanted selectively with boron ions to create p-type regions as sensing resistors and p+ regions for interconnection;

FIGURE 2D shows the wafer of FIGURE 2C after etching to form p+ interconnections and p-type sensing resistors;

FIGURE 2E shows the wafer of FIGURE 2D with an additional nitride deposition and etching;

FIGURE 2F schematically illustrates in a cross-sectional side view the pressure sensor of FIGURE 1 in an etching fixture for etching the silicon substrate;

FIGURE 3 illustrates a cross-sectional view of another embodiment of a pressure sensor constructed in accordance with the invention;

FIGURE 3A shows a cross-sectional view of a silicon substrate wafer with external masking to produce a localized, buried silicon oxide volume;

FIGURE 3B shows the wafer of FIGURE 3A with additional epitaxial silicon growth; and

FIGURE 3C shows the wafer of FIGURE 3B with additional oxygen ion implantation and annealing to create a silicon oxide dielectric layer with surface silicon.

Description of Illustrated Embodiments

[0018] Generally, FIGURES 1 and 1A show a semiconductor pressure sensor 10 constructed in accordance with the invention; and FIGURES 2-2F illustrate the manufacturing stages to fabricate the sensor 10 beginning with a common silicon-on insulator (SOI) wafer.

[0019] In particular, the sensor 10 has a single-crystal diaphragm 14 made of epitaxially grown single-crystal silicon disposed between single-crystal p-type gage elements 18 and a silicon substrate 12. The substrate 12 includes a localized region of oxygen ion implantation to form a silicon oxide layer 16, which functions as a dielectric isolator and as an etch stop for when the substrate 12 is etched to form the pressure port 32. The single-crystal silicon diaphragm 14 is disposed between the oxide layer 16 and another oxide layer 17. Layer 17 serves as a dielectric isolator to isolate one gage element 18 from other gage elements 18, and from the diaphragm 14 and the substrate 12. The sensor 10 is annealed and implanted with boron ions, in selected localized regions, and selectively etched, to form the gage elements 18 as p-type gage piezoresistors and p+ interconnections 20. A nitride deposition layer 22 preferably passivates the p-type piezoresistors 18. Metal contacts 24 provide electrical communication to the p+ interconnections 20 and provide a way to externally connect the sensor 10 to a further electrical device.

[0020] The electrical signals produced at the metal contacts 24 are an indication of the pressure differential across the diaphragm 14, i.e., between pressure environments 28 and 30. More particularly, the electrical signals at the contacts 24 are produced by the p-type gage elements 18 and are indicative of a resistance change functionally dependent upon the stress of the diaphragm 14. The etched portion 31 of the substrate 12 defines a pyramidal pressure port 32, which exposes the diaphragm 14 to the pressure environment 28, and the substrate 12 supports the sensor 10 at a header interface, e.g., at the mounting headers 26.

[0021] The FIGURE 1 showing of the pressure sensor 10, and the similar drawings in FIGURES 2-3, contain exaggerated proportions for clarity of illustration. For example, the silicon oxide layer 16, FIGURE 1, is typically 0.45 micron thick, and the etched piezoresistive gage elements 18 are typically 0.4 micron thick.

[0022] FIGURE 1A is a diagrammatic top view (not to scale) of the sensor 10 of FIGURE 1, showing the p+ interconnections 20 and the p-type piezoresistive elements 18. The gage elements 18, which preferably interconnect and form a conventional Wheatstone bridge configuration at the inner ends of the p+ interconnections 20, are located over the edges of the pressure port

32, as defined by the edge of the substrate silicon etched portion 31 (FIGURE 1). The metal contacts 24, for connecting the sensor 10 to an external electronic device, are located at the outer ends of the p+ interconnections 20. A disturbance to this bridge circuit, caused by pressure-induced diaphragm deflection, provides a measurable voltage signal at the contacts 24.

[0023] In order to produce maximal additive read-out of diaphragm movement, the gage elements 18 are preferably oriented in a push-pull configuration. In this configuration, each of the elements 18 is oriented relative to the edge of the diaphragm 14 that is nearest to the element, with two of the elements 18 arranged perpendicular to the edge, and the other two elements arranged parallel to the edge.

[0024] The sensor 10 can include aluminum bond pads 34, 35 which, for clarity of illustration, are only shown in FIGURE 1A. These pads connect electrically to the contacts 24 and provide a durable and convenient forum for connecting external electronics, e.g., wires, to the sensor to acquire the electrical signal from the semiconductor interconnections 20. Typically, the pads 34 are connected to a voltage source, and the pads 35 provide a measurement signal indicative of pressure on the diaphragm 14.

[0025] FIGURE 2 illustrates a general silicon-on-insulator (SOI) wafer 40 that has a silicon substrate 12 implanted with oxygen ions to create a buried silicon oxide layer 16 which typically is approximately 0.45 micron thick. Ion implantation is a known process and usually includes an ion source, focusing elements, an acceleration tube and a mass analyzer. The silicon oxide layer 16 can be formed very precisely with known technologies and forms a dielectric isolator which inhibits leakage between subsequently-formed piezoresistive gage elements. A single-crystal silicon layer 42 is formed on the silicon oxide layer 16 by an annealing process, also well known, to a thickness typically of approximately 0.2 to 0.4 micron. Surface silicon annealing typically occurs over one to two hours in a dry nitrogen environment at a temperature over 1000°C.

[0026] The SOI wafer 40 of FIGURE 2, formed by oxygen ion implantation and annealing, is commercially available. The SOI structure provides improved dielectric isolation when combined with further features of the invention. Further, the practice of the invention is not limited to the implanted silicon oxide layer 16 of FIGURES 1, 1A and 2; other silicon oxide forms are acceptable as dielectric isolators.

[0027] To fabricate the sensor 10 of FIGURE 1 from the wafer 40 of FIGURE 2, and as shown in FIGURE 2A, the surface silicon layer is grown to an additional thickness of approximately one to fifteen microns with epitaxial single-crystal silicon to form the diaphragm 14. After the desired diaphragm thickness is achieved, the wafer of FIGURE 2A is again implanted with oxygen ions to form a silicon oxide implantation 17, and annealed to create surface silicon 25, as shown in FIGURE 2B.

[0028] The SOI wafer of FIGURE 2B is selectively doped with boron ions 46, as illustrated in FIGURE 2C, at the single-crystal silicon surface layer 25, to prepare for the formation of p-type piezoresistive gage elements and of p+ interconnections. The piezoresistive gage elements 18 and interconnections 20 are formed by etching the doped single-crystal silicon, as illustrated in FIGURE 2D. Preferably, but not required, nitride deposition forms a passivation layer 22, as shown in FIGURE 2E. The passivation layer 22 is functionally used to electrically insulate the p-type gage elements 18 from other elements of the sensor 10 (FIGURE 1). Selective etching of the layer 22 provides access for the contact 24 shown in FIGURE 2F.

[0029] FIGURE 2F illustrates a final step in the illustrated embodiment for producing the sensor 10 of FIGURE 1. In particular, the silicon substrate 12 is etched with an appropriate etchant at the illustratively pyramidal etch region 31, while the front of the sensor, e.g., the gage elements 18 are protected from the etchant by a conventional fixture 50, illustrated as having an O-ring interface seal 52. The metals contact 24 are formed by evaporated aluminum deposition and etching on each p+ interconnection 20. Other high temperature metals can also be used for the interconnections.

[0030] Alternative to the embodiment described above, the sensor 10 of FIGURE 1 can exclude the step of implanting the silicon oxide layer 16, and can form the pressure port 32 by controlled etchant timing. According to this alternative embodiment, the SOI wafer of FIGURE 2 is implanted with boron ions, similar to the FIGURE 2B description, to create p-type gage elements 18 and p+ interconnections 20. Epitaxial single-crystal silicon is grown directly on the substrate to form a diaphragm portion, whereafter the substrate is etched by controlled timing to the epitaxial silicon layer. The resultant sensor has the same structure as shown in FIGURE 1, except it lacks the isolation layer 16, and has the same electrical representation as shown in FIGURE 1A.

[0031] A sensor 100 shown in FIGURE 3 illustrates another embodiment in accordance with the invention. FIGURES 3A-3C illustrate steps to manufacture the sensor 100.

[0032] An etched substrate 12" forms both a diaphragm 102 and an over-range cavity protection region 104 in the sensor 100. The diaphragm 102 has a dielectric silicon oxide implantation layer 16" to isolate one piezoresistive gage element 18" from other elements of the sensor 100. P+ interconnections 20" are given electrical passage to areas external to the sensor 100 via metal contacts 24". Preferably, a nitride deposition 22" passivates the gage elements 18", providing additional dielectric isolation.

[0033] The over-range cavity protection region 104 is created by forming a localized volume of silicon oxide, as illustrated in FIGURE 3A, with a depth of approximately 0.5 to 1 micron by ion implantation. A metal mask 110 shields the substrate 12" while oxygen ions 112 are

focused at the over-range region 104. Then, as shown in FIGURE 3B, epitaxial single-crystal silicon is grown on the surface silicon area, which is part of the substrate 12", and above the over-range cavity protection region 104. The diaphragm 102 is implanted with oxygen ions and annealed to form a dielectric silicon oxide layer 16", shown in FIGURE 3C, and a surface silicon layer 103, which is selectively doped with boron ions for the gage elements 18" and for the p+ interconnections 20" of FIGURE 3. Etchant, e.g., potassium hydroxide, is used to remove the silicon of the base substrate 12", within a pyramidal volume bounded by dashed lines 114 of FIGURE 3C, up to the stop created by the localized silicon oxide volume at the over-range cavity protection region 104. Another etchant, e.g., hydrofluoric acid, is then used to remove the silicon oxide localized volume, creating an over-range cavity protection region 104. Over-range cavity protection helps to ensure that the diaphragm is not over-stressed between extreme pressure environments; i.e., if the diaphragm 102 is subjected to a pressure differential that would over-stress it, the deflected diaphragm abuts the substrate 12" at the over-range cavity protection region 104, thereby avoiding damaging, over-deflection.

[0034] Preferably, the metal contacts 24" of FIGURE 3 are connected to lead-out pads, e.g., the aluminum bond pads 34, 35 of FIGURE 1A, to assist in external packaging and connection to the sensor 100.

[0035] Those skilled in the art will appreciate that modifications to the above description, and to the illustrated structures and procedures can be made without departing from the spirit and scope of the invention. For example, the sensor 10 of FIGURE 1 is readily configured to external lead-out pads, and connected to a Wheatstone bridge configuration as is well-known to those skilled in the art. Further, and without limitation, layer thicknesses and multiple oxygen ion implantations, as illustrated in FIGURES 1-3, can be changed or implemented through a variety of means known in the semiconductor fabrication art.

[0036] It is thus seen that the invention efficiently attains the objects set forth above, among those apparent in the preceding description. In particular, the invention provides a high sensitivity semiconductor pressure sensor with relatively high temperature stability. It also provides sensors with etch stop capability and with over-range cavity protection, and it provides sequences of steps for the manufacture of such sensors.

[0037] It is accordingly intended that all matter contained in the above description or shown in the accompanying drawings be interpreted as illustrative, rather than as limiting.

[0038] It is also understood that the following claims are to cover all specific and generic features of the invention as described herein, and all the statements of the scope of the invention.

Claims

1. A method for manufacturing a semiconductor pressure sensor (10), said method comprising the successive steps of

(A) providing a silicon-on-insulator wafer, said wafer including a silicon substrate (12), a first silicon oxide implantation (16) for forming an etch stop, and a first surface annealed silicon (42),

(B) epitaxially growing additional single-crystal silicon (14) on said first surface silicon for forming a diaphragm with opposing first and second surfaces,

(C) implanting oxygen ions in said additional single-crystal silicon for forming a dielectric isolator (17),

(D) annealing said implanted additional single-crystal silicon thereby forming a second surface silicon on said dielectric isolator (25),

(E) forming a dielectrically isolated single-crystal silicon piezoresistive gage element (46) in said second surface silicon by boron ion implantation and etching,

(F) forming an external connector (20) by metal evaporation and etching, said external connector being in circuit with said gage element for providing an external electrical connection to said sensor, and

(G) etching said substrate to said etch stop such that said diaphragm can deflect in response to a pressure difference between said first and second surfaces.

2. A method according to claim 1 comprising the further step of depositing passivation nitride (22) on said piezoresistive gage element, after said step of forming a dielectrically isolated single-crystal piezoresistive gage element, for providing additional dielectric isolation of said gage element.

3. A method according to claims 1 and 2, wherein said first silicon oxide implantation (104) is confined to a localized volume in said substrate, and comprising the further steps of etching said first silicon oxide implantation at said localized volume for forming an over-range cavity protection region.

Patentansprüche

1. Verfahren zum Herstellen eines Halbleiterdrucksensors (10), mit den folgenden Schritten:

(A) Bereitstellen eines Wafers mit Silizium-auf-Isolatoraufbau, wobei der Wafer ein Siliziumsubstrat (12), eine erste Siliziumoxidimplantierung (16) zur Ausbildung eines Ätzstops und eine erste Oberfläche mit geglühtem Silizium (42) enthält, 10

(B) epitaktisches Aufwachsen von zusätzlichem einkristallinem Silizium (14) auf dem Silizium der ersten Oberfläche für die Ausbildung einer Membran, die sich gegenüberliegende erste und zweite Oberflächen aufweist, 15

(C) Implantieren von Sauerstoffionen in das zusätzliche einkristalline Silizium für die Ausbildung eines dielektrischen Isolators (17)

(D) Glühen des implantierten zusätzlichen einkristallinen Siliziums, um hierdurch ein zweites Oberflächensilizium auf dem dielektrischem Isolator (25) zu bilden, 20

(E) Ausbilden eines dielektrisch isolierten, aus einkristallinem Silizium bestehenden piezoresistiven Fühlerelements (46) in dem zweiten Oberflächensilizium durch Implantieren von Borionen und Ätzen, 25

(F) Ausbilden eines externen Verbinders (20) durch Aufdampfen von Metall und Ätzen, wobei der externe Verbinder mit dem Fühlerelement zur Herstellung eines externen elektrischen Anschlusses an den Sensor verbunden ist, und 30

(G) Ätzen des Substrats bis zu dem Ätzstop derart, daß die Membran als Reaktion auf eine Druckdifferenz zwischen der ersten und der zweiten Oberfläche ausgelenkt werden kann. 35

2. Verfahren nach Anspruch 1, mit dem weiteren Schritt des Aufbringens von passivierendem Nitrid (22) auf dem piezoresistiven Fühlerelement nach dem Schritt des Ausbildens eines dielektrisch isolierten, aus einkristallinem Silizium bestehenden piezoresistiven Fühlerelements, um hierdurch eine zusätzliche dielektrische Isolierung des Fühlerelements zu schaffen. 40 45

3. Verfahren nach den Ansprüchen 1 und 2, bei dem die erste Siliziumoxidimplantierung (104) auf ein lokalisiertes Volumen in dem Substrat beschränkt ist, und das die weiteren Schritte des Ätzens der ersten Siliziumoxidimplantierung bei dem lokalisierten Volumen zur Ausbildung einer Bereichsüberschreitungs-Hohlraum-Schutzregion umfaßt. 50 55

Revendications

1. Un procédé de fabrication d'un capteur de pression à semi-conducteur (10), ce procédé comprenant les étapes successives consistant à :

(A) fournir une tranche de silicium sur isolant, cette tranche comprenant un substrat de silicium (12), une première implantation d'oxyde de silicium (16) pour former une limite de gravure chimique, et un premier silicium (42) recuit en surface,

(B) faire croître par épitaxie du silicium monocristallin (14) supplémentaire sur le premier silicium de surface, pour former une membrane ayant des première et deuxième surfaces opposées,

(C) implanter des ions oxygène dans le silicium monocristallin supplémentaire pour former un isolant diélectrique (17),

(D) exposer à un recuit le silicium monocristallin supplémentaire implanté, formant de ce fait un deuxième silicium de surface sur l'isolant diélectrique (25),

(E) former une jauge de contrainte piézorésistive (40) en silicium monocristallin, isolée diélectriquement, dans le deuxième silicium de surface par une implantation d'ions de bore et une gravure chimique,

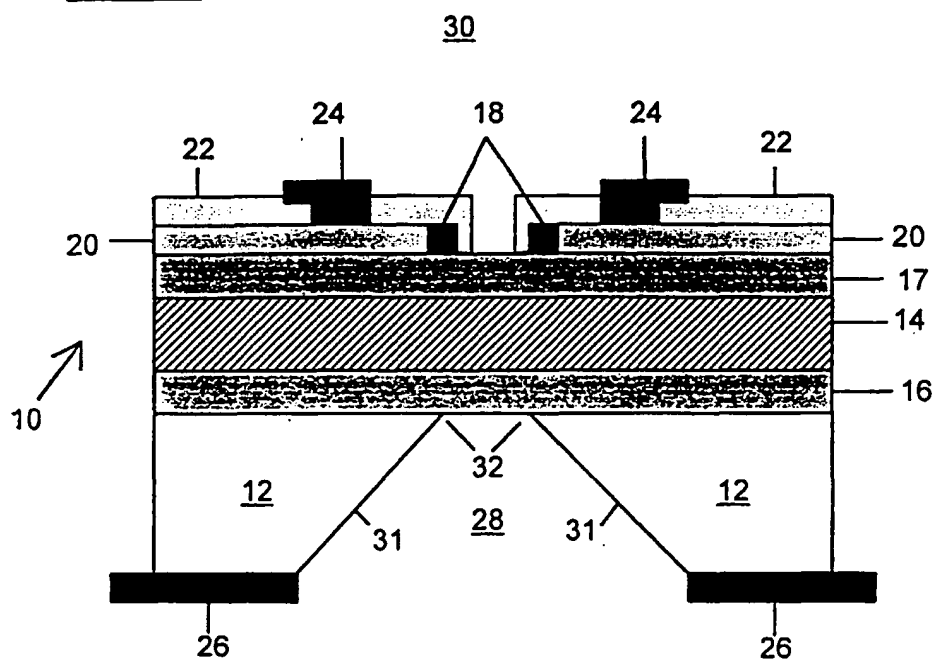
(F) former un connecteur extérieur (20) par une évaporation de métal et une gravure chimique, ce connecteur extérieur étant en circuit avec la jauge de contrainte pour former une liaison électrique extérieure au capteur, et

(G) graver chimiquement le substrat pour la limite de gravure chimique, de façon que la membrane puisse se déformer en réponse à une différence de pression agissant entre les première et deuxième surfaces.

2. Un procédé selon la revendication 1, comprenant l'étape supplémentaire de dépôt de nitrure de passivation (22) sur la jauge de contrainte piézorésistive, après l'étape de formation de cette jauge de monocristalline, isolée diélectriquement, pour fournir une isolation diélectrique supplémentaire à la jauge.

3. Un procédé selon les revendications 1 et 2, dans lequel la première implantation d'oxyde de silicium (104) est confinée à un volume localisé dans le substrat et comprend les étapes supplémentaires de gravure chimique de la première implantation d'oxyde de silicium sur le volume localisé, pour former une zone de protection de cavité.

FIGURE 1



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FIGURE 1A

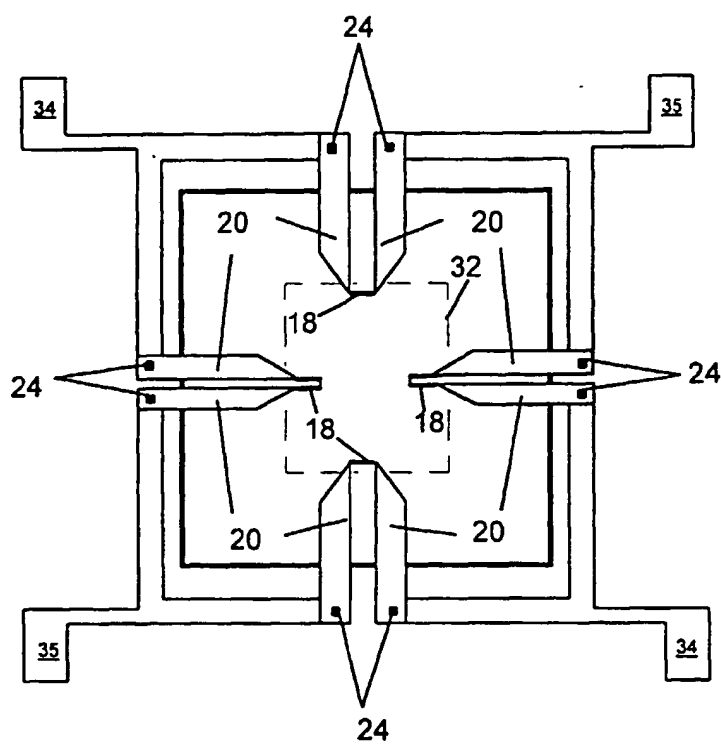


FIGURE 2

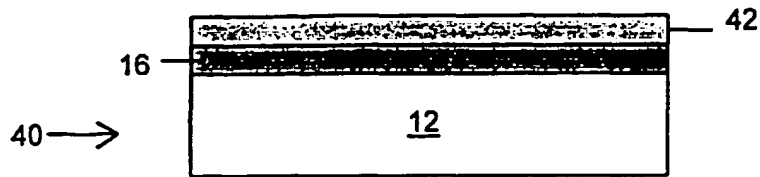


FIGURE 2A

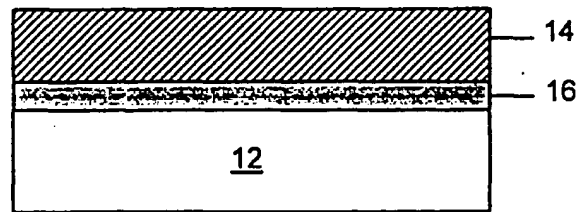


FIGURE 2B

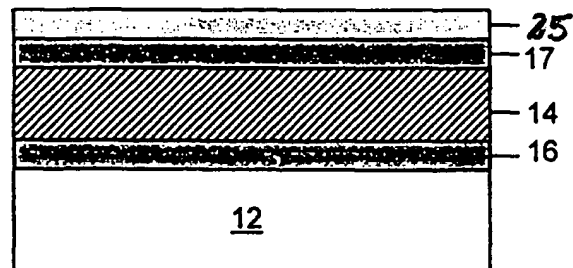


FIGURE 2C

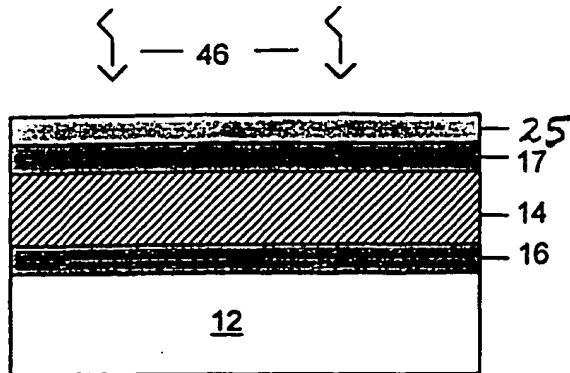


FIGURE 2D

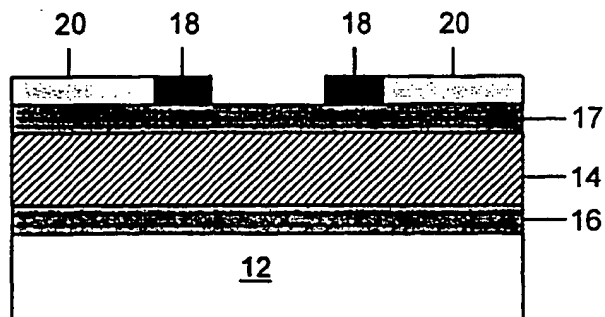
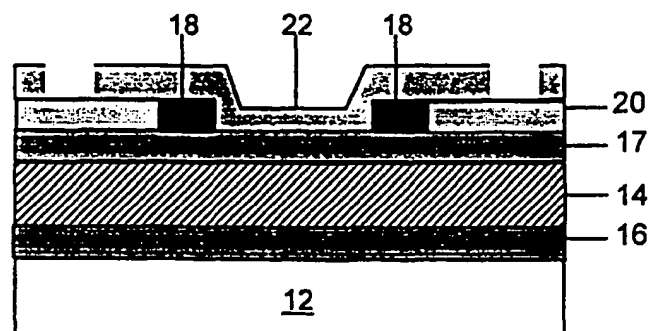


FIGURE 2E



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FIGURE 2F

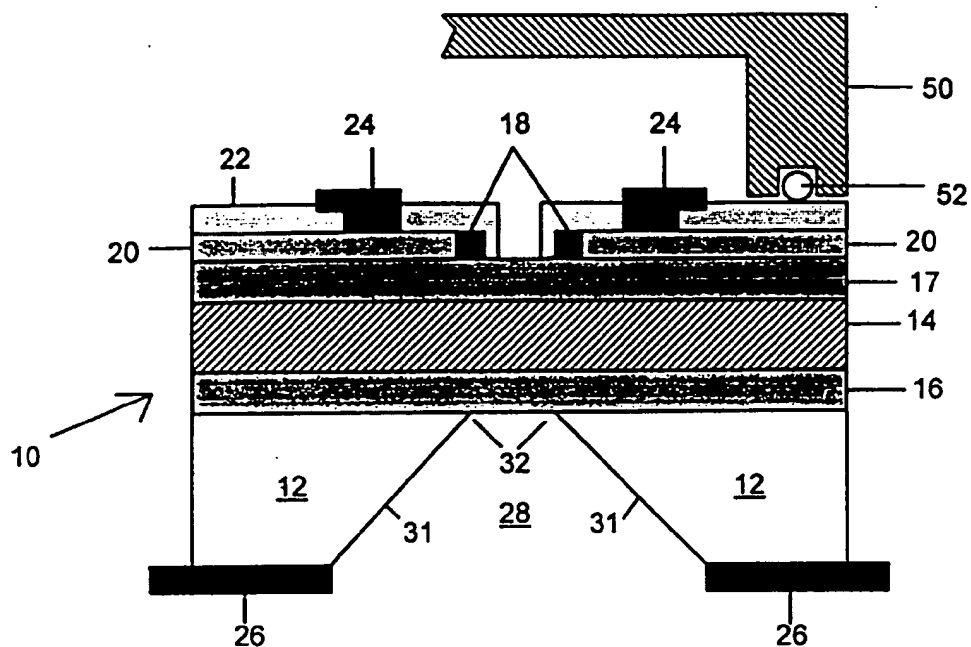


FIGURE 3

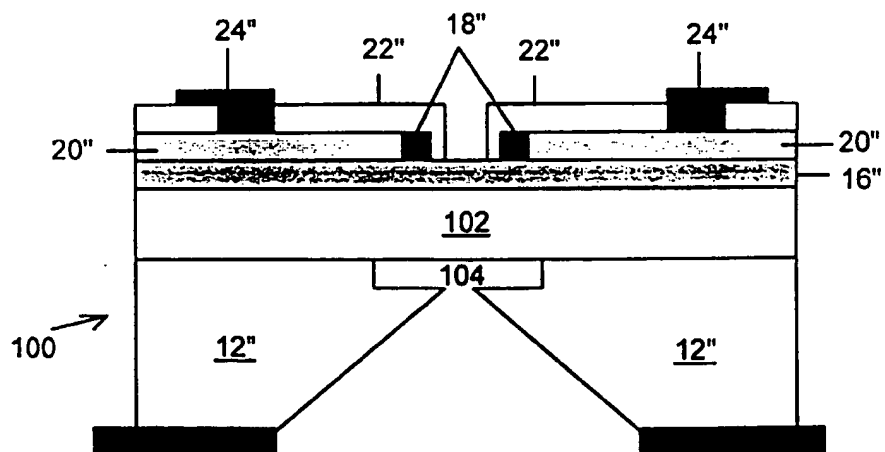


FIGURE 3A

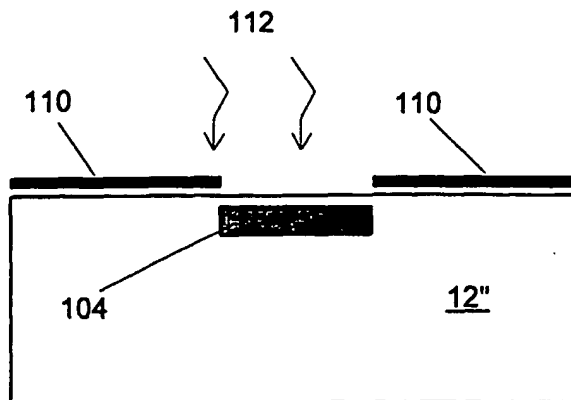


FIGURE 3B

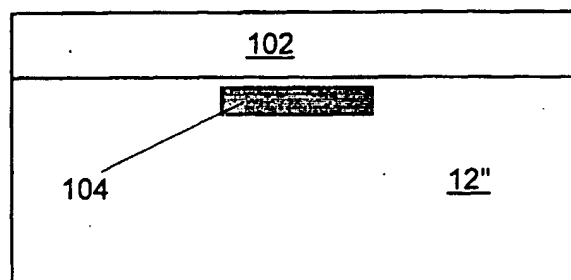
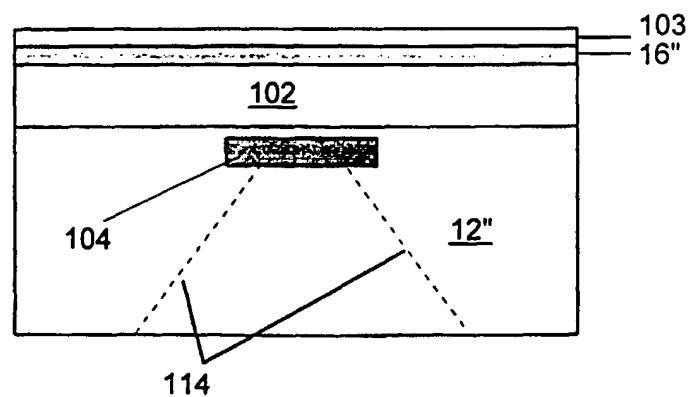


FIGURE 3C



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